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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/211,677	12/14/1998	HYUN CHANG LEE	8733D-7153	9588

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EXAMINER
NGUYEN, KEVIN M

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 07/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/211,677	LEE, HYUN CHANG	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on 5/15/2003 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 27-81 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 27-81 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/15/2003 has been entered. An action on the RCE follows:

Allowable Subject Matter

2. The indicated allowability of claims 27-37 and 51-55 are withdrawn in view of the newly discovered reference(s) to Yasui et al (US 5,784,039) in view Kubota et al (US 5,754,155). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 27-33, 36-46, 49-63 and 65-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al (US 5,784,039) in view of Kubota et al (US 5,754,155).

5. **As to claims 27 and 51**, Yasui et al teach an active matrix liquid crystal display apparatus associate a method, comprising: a pixel 4, a switching transistor Qij, a data

signal line S1, a gate signal line G1, a data driver 2, a gate driver 3, a first voltage source V_{GH}, a second voltage source V_{GL} (see figures 1A and 1B), a switch Swi (figure 7), a gate controller 3 (see figure 6C);

the gate controller 3 applies gate control signal that cause the gate driver 3 to apply the first voltage V_{GH} to the gate signal line Gi (see figure 3A);

the gate controller 3 applies gate control signal that cause the gate driver 3 to apply the second voltage V_{GL} to the gate signal line Gi after the application of the first signal voltage (see figure 3B);

Yasui et al fail to teach applying a reference potential to the gate signal line after the application of the second signal voltage. However, Kubota et al teach a related active matrix liquid crystal display apparatus which includes applying the reference voltage ($V_{GH'}$, $V_{GL'}$) (12a) to the gate signal line after the application of the second signal voltage (V_{GH} V_{GL}) (see figure 2, column 9, lines 53-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the reference voltage circuit ($V_{GH'}$, $V_{GL'}$)(12a) after the application of the second signal voltage (V_{GH},V_{GL}) taught by Kubota et al for the gate voltage source (V_{GH}, V_{GL}) disclosed in the TFT-LCD device of Yasui et al because this would display an image with high quality and excellent ability while fabricating a gate driver lower prices (column 6, lines 5-8 of Kubota et al).

6. **As to claim 38**, Yasui et al teach a liquid crystal display device, comprising: a plurality of pixels 4, a switching transistor Qij, a plurality of data signal lines S1...Sn, a plurality of scanning signal lines G1...Gm+1, a data driver 2, a gate driver 3, a first

voltage source V_{GH}, a second voltage source V_{GL} (see figures 1A and 1B), a plurality of switches Swi to Swi+n (figure 7), a gate driver 3 (see figure 6C);

the gate driver (3) outputs the first voltage V_{GH} on a selected gate line during the application of a data signal in response to a scanning clock signal $-t_0<t<t_1$ (see figure 3A);

the gate driver (3) outputs the second voltage V_{GL} on a selected gate line during the application of a data signal in response to a scanning clock signal $t_1<t<t_2$ (see figure 3B);

Yasui et al fail to teach the gate driver outputs a applying a reference potential after the application of the second signal voltage. However, Kubota et al teach a related LCD device which includes applying the reference voltage ($V_{GH'}$, $V_{GL'}$) (12a) to the gate signal line after the application of the second signal voltage (V_{GH} V_{GL}) (see figure 2, column 9, lines 53-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the reference voltage circuit ($V_{GH'}$, $V_{GL'}$)(12a) after the application of the second signal voltage (V_{GH}, V_{GL}) taught by Kubota et al for the gate voltage source (V_{GH}, V_{GL}) disclosed in the LCD device of Yasui et al because this would display an image with high quality and excellent ability while fabricating a gate driver lower prices (column 6, lines 5-8 of Kubota et al).

7. **As to claims 56, 62, 71 and 76,** Yasui et al teach an active matrix liquid crystal display device associate a method, comprising: a plurality of pixels 4, a switching transistor Qij, a plurality of data signal lines S1...Sn, a plurality of gate signal lines G1...Gm+1, a data driver 2, a gate driver 3, a first voltage source V_{GH}, a second voltage

source V_{GL} (see figures 1A and 1B), a plurality of switches Swi to Swi+n (figure 7), a gate driver 3 (see figure 6C);

the gate driver (3) receiving the first voltage V_{GH} on a selected gate line during the application of a data signal in response to a scanning clock signal $-t_0<t<t_1$ (see figure 3A);

the gate driver (3) receiving the second voltage V_{GL} on a selected gate line during the application of a data signal in response to a scanning clock signal $t_1<t<t_2$ (see figure 3B);

Yasui et al fail to teach "said first gate voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching transistor prior to transition to the second gate voltage, wherein the second gate voltage has a voltage level that turns off the switching transistor." However, Kubota et al teach a related active matrix liquid crystal display apparatus which includes

$V_{GH'} > V_{sat} + V_{on(PIX)}$ by only $V_{th(PIX)}$

$V_{GL'} > -V_{sat} - V_{off(PIX)}$ by only $V_{th(PIX)}$

relying to the claimed limitation the first gate voltage $V_{sat} + V_{on(PIX)}$ reducing a voltage level substantially to a threshold voltage level $V_{th(PIX)}$ but enough to maintain an on-state $V_{on(PIX)}$ of the switching transistor $TR_{(PIX)}$ prior to transition to the second gate voltage $-V_{sat} - V_{on(PIX)}$, wherein the second gate voltage $-V_{sat} - V_{on(PIX)}$ has a voltage level that turns off $V_{off(PIX)}$ the switching transistor $TR_{(PIX)}$ (see figure 2, column 9, lines 20-30).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize $V_{GH'} > V_{sat} + V_{on(PIX)}$ by only $V_{th(PIX)}$ and $V_{GL'} > -V_{sat} - V_{off(PIX)}$ by only $V_{th(PIX)}$ taught by Kubota et al for the gate voltage source (V_{GH}, V_{GL}) disclosed in the TFT-LCD device of Yasui et al because this would display an image with high quality and excellent ability while fabricating a gate driver lower prices (column 6, lines 5-8 of Kubota et al).

As to claims 28, 41, 57, Yasui et al teach the gate signal line has a potential that drops from the first voltage to the second voltage over a period of time (see figure 4A).

As to claims 29, 42, 53, 58, 78, Yasui et al teach the gate signal line drops exponentially over the period of time (t_7 to t_8) (see figure 9).

As to claims 30, 43, 54, 59, 79, Yasui et al teach the gate signal line drops linearly over the period of time (see figure 4A).

As to claims 31, 44, 55, 60, 80, Yasui et al teach the gate signal line drops stepwise (dV_P, dV_Q) over the period of time from t_1 to t_6 (see figure 10).

As to claims 32, 45, 52, 61, 77, Yasui et al teach the first voltage (V_{GH}) is greater than a second voltage (V_{GL}) (see figure 10).

As to claims 33, 46, Yasui et al teach the gate controller 3 including a timing controller (t).

As to claims 36, 49, Yasui et al teach the first voltage is applied before the data signal is applied (see figure 3A).

As to claims 37, 50, Yasui et al teach the second voltage (V_{GL}) is ground (see figure 3A).

As to claim 39, Yasui et al teach the gate driver 3 sequentially changed the selected gate line Gi (see figure 3).

As to claim 40, Yasui et al teach the gate driver 3 includes a switch SWi that selectively provides the first voltage and the second voltage to the selected gate line (see figure 7).

As to claim 63, Yasui et al teach the first gate voltage V_{GH} is supplied to the gate lines Gi during a time interval –t0<t<t1 when the thin film transistors TFT connected to the gate lines are turned on (see figure 3A).

As to claims 65, 68, 69, 70, 81, Kubota et al teach the first gate voltage V_{sat} + $V_{on(PIX)}$ reducing a voltage level substantially to a threshold voltage level $V_{th(PIX)}$ prior to excitation of successive gate signal line (see figure 2).

As to claims 66, 67, 72-75, Yasui et al teach a voltage controller comprising the switch Swi (see figure 7) and a low level gate voltage generator $-V_{sat} - V_{off(PIX)}$, and switch $TR_{(PIX)}$ (see figure 2).

8. Claims 35 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al in view Kubota et al, and further in view of Applicant's Admitted Prior Art hereinafter AAPA.

As to claims 35 and 48, Yasui et al and Kubota et al teach all of the claimed limitation of claims 27 and 38, except for the gate signal line includes a distributed series resistance and a distributed capacitance. However, AAPA discloses the gate signal line includes a distributed series resistance R1 and a distributed capacitance C1 (see figure 3, page 5, lines 2-5). Since a waveform modifying circuit such as an

integrator for each gate line must be added (page 5, lines 30-32). Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the gate signal line includes a distributed series resistance R1 and a distributed capacitance C1 disclosed by AAPA in Yasui et al's scanning line of TFT-LCD device because this would eliminate flickering and residual image (see page 5, lines 29-30 of AAPA).

9. Claims 34, 47 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al in view Kubota et al, and further in view of Hirai et al (US 5,646,643).

As to claims 34, 47 and 64, Yasui et al and Kubota et al teach all of the claimed limitation of claims 27, 38 and 62, except for the shift register. However, Hirai et al teach a register 707 controlling the switching section 709 (see figure 8). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize a register 707 taught by Hirai et al in Yasui et al's and Kubota et al's gate driver because this would provide high grade of image display by a simple and inexpensive means of solving a drawback of display fluctuation or crosstalk on a display in the LCD device (column 8, lines 32-35 of Hirai et al).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Examiner
Art Unit 2674

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600